What is Claimed is:

1. A memory unit comprising:
a memory portion having storage units storing data bits;
a memory portion storing error correction bits;
an error checking and correction unit; and
registers to hold the location of one or more corrected bits.

2. The memory unit as recited in claim 1 wherein the error checking and correction unit includes circuitry for requesting an interrupt and/or for setting a flag which can be polled, when a failing bit can be corrected.

3. The memory unit as recited in claim 1 wherein the error detection and correction unit includes circuitry for requesting an abort condition when a failing bit is detected which can not be corrected.

4. The memory unit as recited in claim 2 wherein the memory is composed of storage units storing data bits that can be set to one of two states, wherein any of the data bits may be changed to a first state independently of the other bits, the resulting state being a programmed state, wherein all of the data bits of a plurality of data bits must be set to the second state simultaneously, the second state being an erased state, the memory unit further comprising:
circuitry to store the location of a correctable error; and
circuitry to generate an interrupt `request;`
circuitry to set a flag bit only when the correctable error is a bit that has been changed from the programmed state to the erased state.

5. A memory unit comprising:

storage units storing data bits;

storage units storing error checking and correction bits; and

an error detection and correction unit wherein the memory unit contains circuitry to optionally exclude the condition where all of the data bits and error detection and correction bits are in the erased state from generating bit correction.

6. A memory unit comprising:

storage units for storing data bits;

storage units for storing error correction bits;

an error detection and correction unit;

circuitry to optionally exclude the condition where all of the data bits and error detection and correction bits are in the programmed state from generating bit correction.

7. A data processing system, the data processing system comprising:

a central processing unit; and

a memory unit, the memory unit including:

a main memory, the main memory storing data signal groups in a plurality of addresses;

an error checking and correction memory, the error checking and correction memory storing error correcting signals for each data signal group in the main memory at the same address in the error checking and correction code memory;

error checking and correction apparatus for identifying and correcting at least one error in a data group accessed by a read operation; and

failing bit apparatus, the failing bit apparatus identifying when a correctable error is the result of a failing location.

8. The data processing system as recited in claim 7 wherein the failing bit apparatus includes:

an address storage unit;

a correction pattern storage unit; and

an interrupt flag unit, the interrupt flag unit issuing an interrupt flag when an error is detected that can be the result of failing bit memory location.

9. The data processing system as recited in claim 8 further comprising an all logic "1"s detection unit for determining whether all of the signals from a main memory and error checking and correction memory are all logic "1".

10. The data processing system as recited in claim 7 wherein the main memory and the error checking and correction memory are implemented in a technology selected from the group consisting of flash technology and EEPROM technology.

11. A method of responding to an error in a signal group retrieved from a non-volatile memory unit, the method comprising:

when the error is correctable, correcting the error in the signal group using error checking and correction techniques; and

when the error is consistent with a failing bit position, restoring the charge associated with the bit position.

12. The method as recited in claim 11 wherein the restoring step includes the steps of:

storing the address of the signal group having the error;

storing the correction pattern identifying location of the error in the signal group; and

providing an interrupt flag to the central processing unit indicating the need to restore a bit location in the memory unit.

13. The method as recited in claim 11 further comprising implementing the main memory and the error checking and correction memory in a technology selected from the group consisting of flash technology and EEPROM technology.

14. A memory unit comprising:

a non-volatile main memory unit;

a non-volatile error memory for storing error checking and correction signals for a signal group in the main memory having the same address;

error checking and correction apparatus, the error apparatus generating a correction pattern identifying the location of an error in an addressed signal group and the associated error signals, the error apparatus generating a restore signal when the error is consistent with a failing bit location;

flag apparatus storing the associated correction pattern and the associated address in response to the restore signal, the flag apparatus generating an interrupt flag in response to the restore signal.

15. The memory unit as recited in claim 14 wherein the stored correction pattern and the stored address are transferred to the central processor for restoration of the failing bit location when the central processing unit services the interrupt.

16. The memory unit as recited in claim 14 wherein the error checking and correction apparatus includes an all logic "1"s detection unit, the all logic "1"s detection unit determining when the signals stored in the main memory and in the error signal memory are all logic "1"s.

17. The memory unit as recited in claim 14 wherein the main memory and the error checking and correction memory are implemented in a technology selected from the group consisting of flash technology and EEPROM technology.